

Y3 CERTIFIED SAFETY CAPACITORS

LS Product Series

NOVACAP is the recognized leader and premier source of safety certified high voltage surface mount capacitors. The LS1808 series was the first to be introduced into the industry and the offering continues to expand.

The LS series is a safety recognized X2Y3 compliant capacitor. The capacitors are manufactured using advanced ceramic and electrode formulation with thin, dense, and precise dielectric layers to satisfy the difficult requirements with unsurpassed quality.

The devices are specifically designed for use in modem, facsimile, telephone and other electronic equipment where lightning or over voltage surges can occur. The devices are offered in the EIA 1808 and 1812 case sizes and in both the COG and X7R dielectrics. The COG is an ultra stable Class I dielectric with negligible dependence of electrical properties on temperature, voltage, frequency and time. They are used in circuitry that require stable performance, high signal transfer integrity, and no surface arcing. The X7R is a stable Class II dielectric with predictable change in properties with temperature, voltage, frequency, and time. The X7R are used in circuitry where capacitor stability and signal transfer integrity are of lower concern. The higher dielectric constant of the X7R ceramic is more prominent to surface arcing. The X7R capacitors may require conformal coating in use to preclude arching over the chip surface.

The devices are compliant with:

- EN 132400 : 1994 + A2 : 1998
- IEC 60384-14 Second Edition : 1993 + A1 : 1995
- IEC 60384-1 Amendment 3 cl 4.14.2 for Resistance to Soldering Heat (cl 4.4)
- IEC 60384-1 Amendment 3 cl 4.34 and 4.35 for Robustness of Terminations (cl 4.3)
- IEC 60384-1 Impulse test made with 2.5KV according to clause 6.4.2.1 in EN 60950
- IEC 60950 creepage distance between live parts of different polarity
- Meets the requirements of EN 61000-4-5, IEC 1000-4-5, IEC 801-4-5 & UL 1950

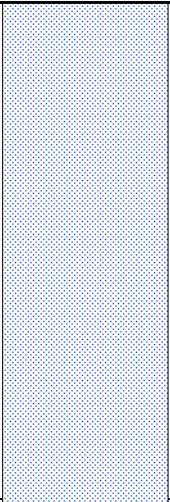
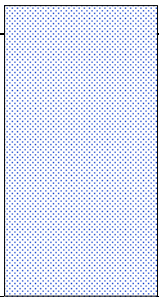
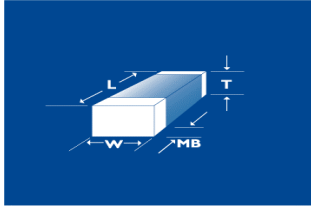

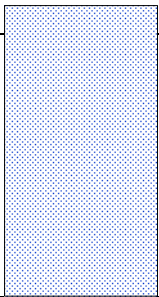

Certification numbers:

- LS1808 (COG): TUV- R9972698.01,.02,.03 UL - NWGQ8.E208336
- LS1812 (COG): TUV- R9972698.05 UL - NWGQ2.E208336
- LS1808 (X7R): TUV- R2272835.01

LS 1808	N	102	K	302	N	X080	T	M
SIZE LS1808 LS1812	DIELECTRIC N=COG B=X7R	CAPACITANCE Two significant figures followed by number of zeros 102=1000pF	TOLERANCE J= +/-5% K= +/-10% M= +/-20%	VOLTAGE-VDCW 302=3000 VDC	TERMINATION N = Nickel Barrier	THICKNESS CODE Not required for .065" Max. Thickness. X080 or X100 required for thickness > .065" See Chart on next page	PACKAGING OPTION T = Reeled	MARKING OPTION Part Marking available upon request

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Capacitance Range: 250VAC (3000VDC)

Size	EIA/IEC 1808	EIA/IEC 1808	EIA/IEC 1812
Length L	.180"±.012 (4.572±0.30)	.180"±.012 (4.572±0.30)	.180"±.012 (4.572±0.30)
Width W	.080"±.008 (2.032±0.20)	.080"±.008 (2.032±0.20)	.125"±.008 (3.175±0.20)
T Max.	.080" (2.032)	.065" (1.651)	.100" (2.540)
MB	.024"±.012 (0.61±0.30)	.024"±.012 (0.61±0.30)	.024"±.012 (0.61±0.30)
Creepage C	.120" min (3.048)	.120" min (3.048)	.120" min (3.048)
Capacitance	COG/NPO	X7R*	COG/NPO
5R0			
6R8			
8R2			
100			
120			
150			
180			
220			
270			
330			
390			
470			
560			
680			
820			
101			
121			
151			
181			
221			
271			
331			
391			
471			
561			
681			
821			
102			
122			
152			
182			
222			

* Capacitors may require conformal coating in use to preclude arcing over the chip surface.



Maximum Thickness of .065". No X065 required in the part number. ie: **LS1808N151K302NT**



Maximum Thickness of .080". X080 required in the part number. ie: **LS1808N102K302NX080T**



Maximum Thickness of .100". X100 required in the part number. ie: **LS1812N202K302NX100T**



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ELECTRICAL CHARACTERISTICS

COG (NPO) Class I Dielectric Capacitors		
Test	Procedure	Requirements
Temperature Coefficient	Operating temperature range -55°C to +125°C	0±30 ppm/°C
Capacitance	1 KHz, 1.0 ± 0.2 VRMS, 25°C 1 MHz for Capacitance < 100pF	Capacitance within specified tolerance
Dissipation Factor	1 KHz, 1.0 ± 0.2 VRMS, 25°C 1 MHz for Capacitance < 100pF	.001 (0.1%) Maximum
Insulation Resistance	After 2 minutes maximum at 750VDC, 25°C	25°C: >100GΩ or >1000ΩF 125°C: >10GΩ or >100ΩF Whichever is less
Impulse Voltage	2.5KV according to EN 60950	No failure shall be observed
Voltage Proof	1500VAC for 60 seconds 2250 VDC for 60 seconds	No permanent breakdown or flashover is permitted.
Capacitance Aging	1 KHz, 1.0 ± 0.2 VRMS, 25°C 1 MHz for Capacitance < 100pF	0% per decade

X7R Class II Dielectric Capacitors		
Test	Procedure	Requirements
Temperature Coefficient	Operating temperature range -55°C to +125°C	±15% Maximum cap change
Capacitance	1 KHz, 1.0 ± 0.2 VRMS, 25°C	Capacitance within specified tolerance
Dissipation Factor	1 KHz, 1.0 ± 0.2 VRMS, 25°C	.025 (2.5%) Maximum
Insulation Resistance	After 2 minutes maximum at 750VDC, 25°C	25°C: >100GΩ or >1000ΩF 125°C: >10GΩ or >100ΩF Whichever is less
Impulse Voltage	2.5KV according to EN 60950	No failure shall be observed
Voltage Proof	1500VAC for 60 seconds 2250 VDC for 60 seconds	No permanent breakdown or flashover is permitted.
Capacitance Aging	1 KHz, 1.0 ± 0.2 VRMS, 25°C 1 MHz for Capacitance < 100pF	<2% per decade

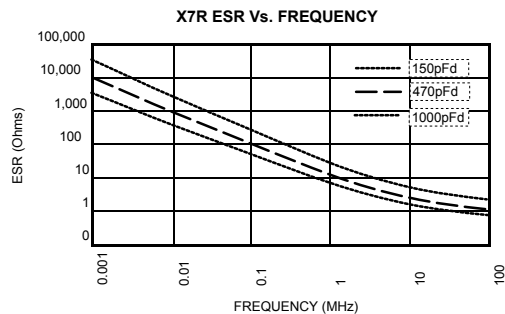
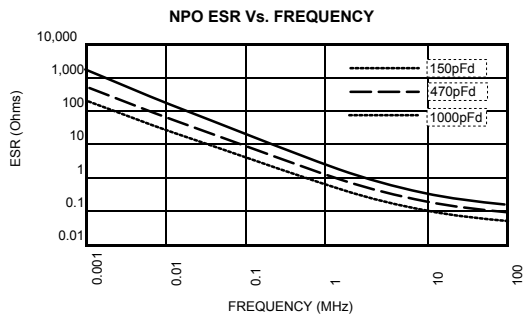
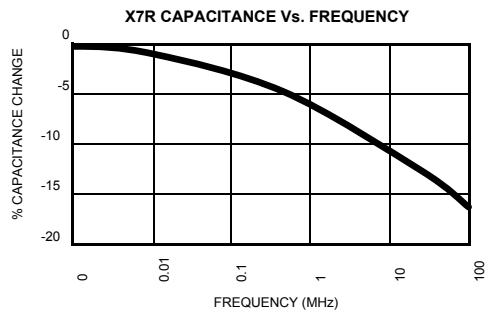
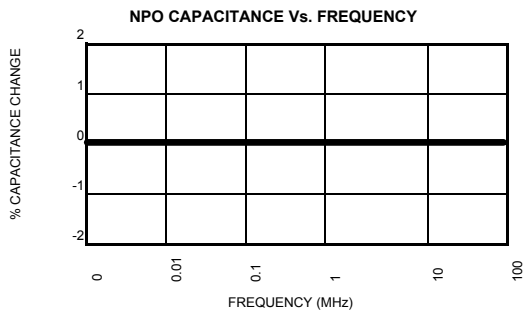
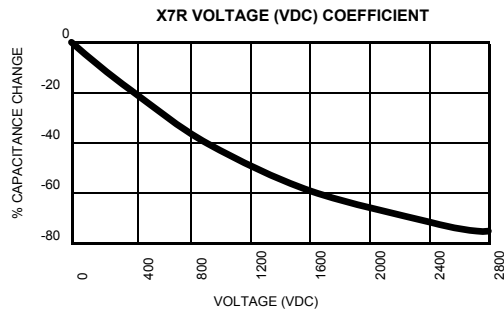
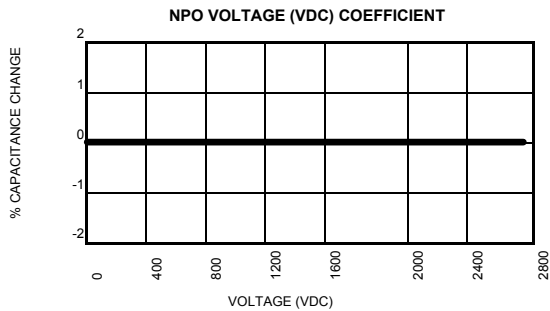
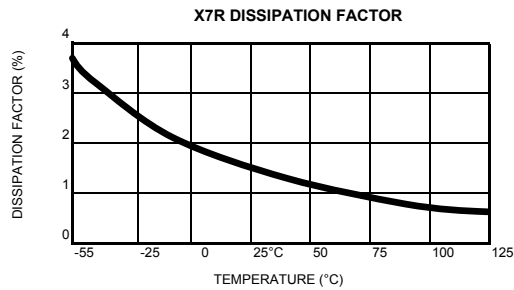
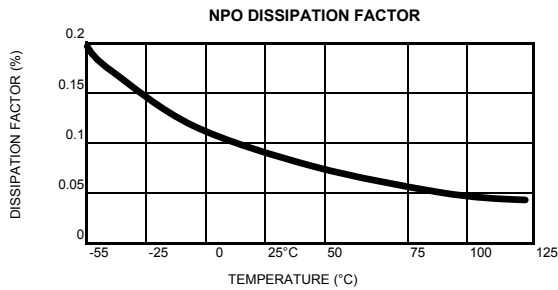
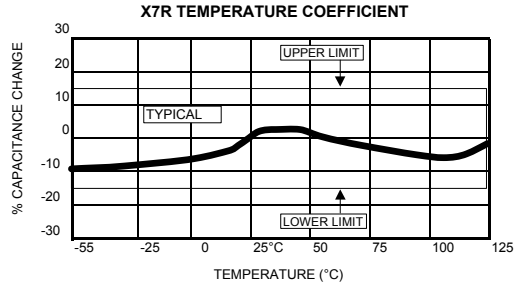
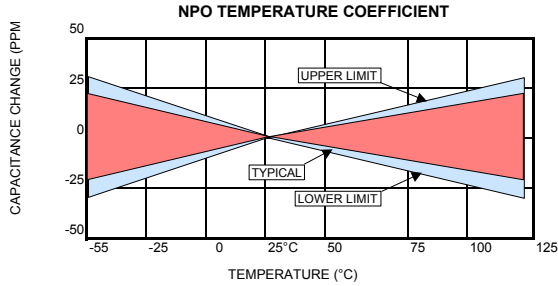
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ENVIRONMENTAL CHARACTERISTICS

Test	Procedure	Requirements
Solderability	MIL-STD-202 Method 208, Test B Sn63 solder at 245±5°C, 5 Seconds	Termination area shall be at least 95% covered with smooth solder coating
Resistance to Soldering Heat	IEC 384-1 cl.4.14 IEC 60384-1, A3: 1989, cl.4.14.2, Method 1. 260°C, 5 Seconds	Termination area shall be at least 75% covered with solder. Delta C <10%
Robustness of Termination (Adhesion)	IEC 60384-1 amendment 3, cl. 4.34 Capacitors mounted on substrate. 5N force applied perpendicular to substrate, parallel to terminations for 10±1 seconds.	No visible damage.
Robustness of Termination (Flex)	IEC 60384-1 amendment 3, cl. 4.35 Capacitors mounted on substrate. Substrate bent by 1mm at a rate of 1mm/s	No visible damage.
Solvent Resistance of Marking	IEC 384-14 cl. 4.20 method 1. Trichlorethylene-Isopropanol mixture for 5 minutes. Rubbing material: cotton wool	The marking shall remain legible after the test.
Damp Heat, Steady State (Humidity)	IEC 384-14 cl. 4.12/IEC384-1 cl.4.22 500 hours at 40±2°C, 90-95% relative on half the samples	No visible damage, Capacitance change <10%, Insulation Resistance > 0.5 X specified value.
Pulse test	EN 60950 cl. 6.4.2.1, 2.5KV. 24 Alternating pulses applied to reflect conditions of EN 60384-14.	No permanent breakdown or flashover is permitted.
Endurance (Life Test)	IEC 384-14 cl. 4.14.3 / 4.14.4 IEC 384-1 cl. 4.23. 1000 hours, 125°C 1.7X rated voltage. Once every hour the voltage shall be increased to 1000 VRMS for 0.1s.	Capacitance change <10%. Insulation Resistance >0.5 X specified value.
Passive Flammability	IEC 384-14 cl.4.17 category C. IEC 384-1 cl.4.38. Needle flame test. 30 seconds.	Burning droplets or glowing parts falling shall not ignite the tissue paper.
Active Flammability	IEC 384-14 cl.4.18 amendment 1. Units wrapped in cheesecloth. 20 pulsed of 2.5KV applied.	No ignition of cheesecloth.

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TYPICAL PERFORMANCE CURVES



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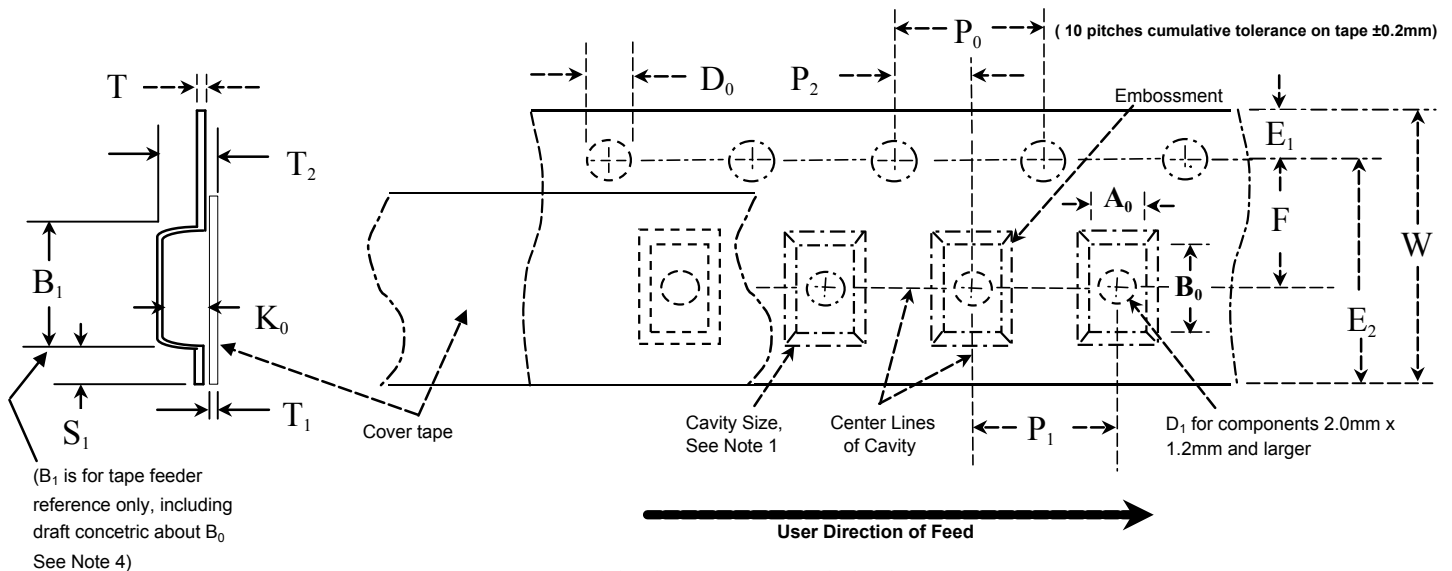
PACKAGING

1) BULK PACKAGE

All NOVACAP capacitors are available in sealed plastic bags. The number of capacitors per bag depends on the thickness and size of the chips.

2) TAPE AND REEL PACKAGE

All tape and reel specifications are in compliance with EIA RS-481. The LS product line utilizes embossed carrier tape. Specify the reeled option (T) in the NOVACAP part number code.



CONSTANT DIMENSIONS

TAPE SIZE	D_0	E_1	P_0	P_2	S_1 MIN.	T MAX.	T_1 MAX.
8mm and 12mm	1.5 +1.10 -0.0	1.75 ±0.10	4.0 ±0.10	2.0 ±0.05	0.8	0.6	0.1

VARIABLE DIMENSIONS

TAPE SIZE	B_1 MAX.	D_1 MIN.	E_2 MIN.	F	P_1 SEE NOTE 5	R MIN. SEE NOTE 2	T_2 MAX.	W MAX.	$A_0 B_0 K_0$
8 mm	4.35	1.0	6.25	3.5 ±0.05	2.0 ±0.05 or 4.0 ±0.10	25	2.5	8.3	See Note 1
12 mm	8.2	1.5	10.25	5.5 ±0.05	2.0 ±0.05 or 4.0 ±0.10 or 8.0 ±0.10	30	6.5	12.3	

Notes:

- The cavity defined by A_0 , B_0 and K_0 shall be configured to provide the following:
 - Surround the component with sufficient clearance such that:
 - the component does not protrude beyond the sealing plane of the cover tape.
 - the component can be removed from the cavity in a vertical direction without mechanical restriction, after the cover tape has been removed.
 - rotation of the component is limited to 20° maximum (see sketches D & E on the next page)
 - lateral movement of the component is restricted to 0.5mm maximum. (see sketch F on the next page)
- Tape with or without components shall pass around radius "R" without damage.
- Bar Code labeling (if required) shall be on the side of the reel opposite the round sprockets holes. Refer to EIA-556.
- B_1 dimension is a reference dimension for tape feeder clearance only.
- If $P_1 = 2.0$ mm, the tape may not properly index in all tape feeders.

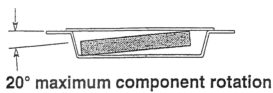
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PACKAGING (Tape Dimensions continued)

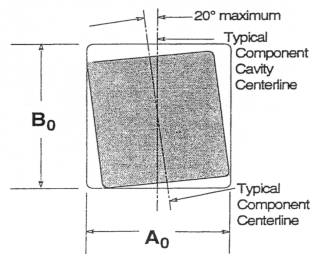
CHIP SIZE	TAPE WIDTH	UNITS PER REEL *	
		7" Diam.	13" Diam.
1808	12mm	2000-3000	10000
1812	12mm	2000-3000	10000

* Quantity per reel varies with chip thickness. Thicker chips (typically higher capacitance values) will result in lesser quantities.

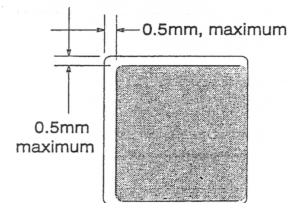
Side or Front Sectional View, Sketch "D"



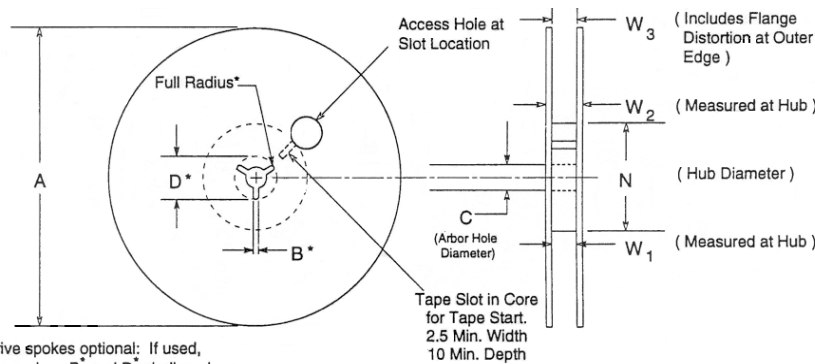
Top View, Sketch "E"
Component Rotation



Top View, Sketch "F"
Component Lateral Movements



REEL DIMENSIONS



* Drive spokes optional: If used, Dimensions B* and D* shall apply.

TAPE SIZE	A MAX.	B* MIN.	C	D* MIN.	N MIN.	W ₁	W ₂ MAX.	W ₃
8 mm	330 (12.992)	1.5 (0.059)	13.0 (+.50 -0.20) (0.512 +.020 -0.008)	20.2 (1.969)	50.0 (1.969)	8.40 (+15 -0.00)	14.4 (0.567)	7.90 Min. (0.311)
						0.331 (+0.059 -0.0)		10.9 Max. (0.429)
12 mm						12.4 (+2.0 -0.0)	18.4 (0.724)	11.9 Min. (0.469)
						0.488 (+0.079 - 0.0)		15.4 Max (0.607)



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SHELF LIFE – STORAGE

Considerations:

The shelf life of ceramic capacitors depends on storage conditions and method of packaging. The ceramic dielectric will not exhibit either intrinsic or extrinsic failures due to shelf storage. The three concerns with ceramic surface mount capacitors in storage are solderability, tape and reel degradation, and aging of class II dielectrics (X7R, Z5U, and Y5V).

The terminations will slowly oxidize with time degrading the solderability. Storage of the capacitors in free air and any contact with either Sulfur Dioxide or Chlorine gas will excel the oxidation of the terminations.

Tape & Reel product should be protected from direct sunlight and used on a “first-in, first-out” basis. All forms of immediate packaging should not be opened until the capacitors are required for use and resealed as soon as practicable.

Class II ceramic capacitors are manufactured with a ferroelectric formulation based on barium titanate. This formulation displays a decay of capacitance with time in any storage condition. This phenomenon is called aging. The loss of capacitance with time is unavoidable with ferroelectric formulation. The aging can be reversed by heating the dielectric above the Curie Point (120°C) and reverting the crystal structure back to its original state. This process can be repeated and will occur during the soldering process.

Storage:

Novacap recommends all products be stored under the following conditions

- 1) Parts are to be stored indoors in the original container.
- 2) Temperature from +5°C to +35°C (41°F to 95°F).
- 3) Relative Humidity between 40% and 75%.

Shelf Life:

Novacap recommends the properly stored ceramic capacitors be used within two years of receipt.

SOLDERING

Soldering methods commonly used in the industry and recommended are Reflow Soldering, Wave Soldering, and to a lesser extent Vapor Phase Soldering. All these methods involve thermal cycling of the components and therefore the rate of heating and cooling must be controlled to preclude thermal shocking of the devices. In general, rates which do not exceed 100° C per minute and a temperature change spike of 100° C maximum for any soldering process is advisable. Other precautions include post soldering handling, primarily avoidance of rapid cooling with contact with heat sinks, such as conveyors or cleaning solutions.

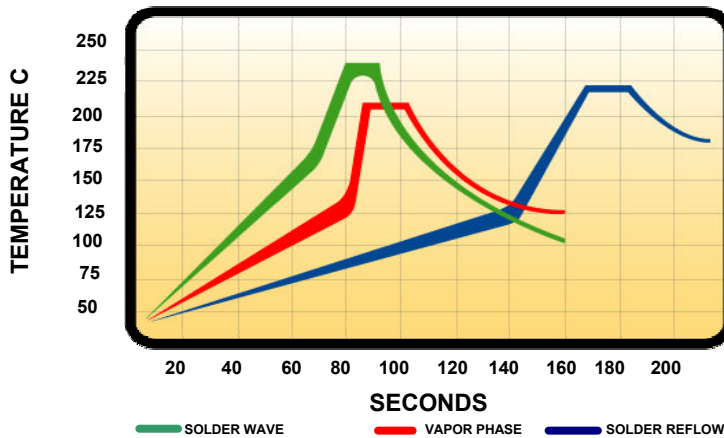
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SOLDERING (continued)

Large chips are more prone to thermal shock as their greater bulk will result in sharper thermal gradients within the device during thermal cycling. Units larger than 1812 experience excessive stress if processed through the fast cycles typical of solder wave or vapor phase operations. Solder reflow is most applicable to the larger chips as the rates of heating and cooling can be slowed within safe limits.

Attachment using a soldering iron requires extra care, particularly with large components, as thermal gradients are not easily controlled and may cause cracking of the chip. Precautions include preheating of the assembly to within 100° C of the solder flow temperature, the use of a fine tip iron which does not exceed 30 watts, and limitation of contact of the iron to the circuit pad areas only.

SOLDER ATTACHMENT RECOMMENDED PROFILES



BOARD DESIGN CONSIDERATIONS

The amount of solder applied to the chip capacitor will influence the reliability of the device. Excessive solder can create thermal and tensile stresses on the component which could lead to fracturing of the chip or the solder joint itself. Insufficient or uneven solder application can result in weak bonds, rotation of the device off line or lifting of one terminal off the pad (tombstoning).

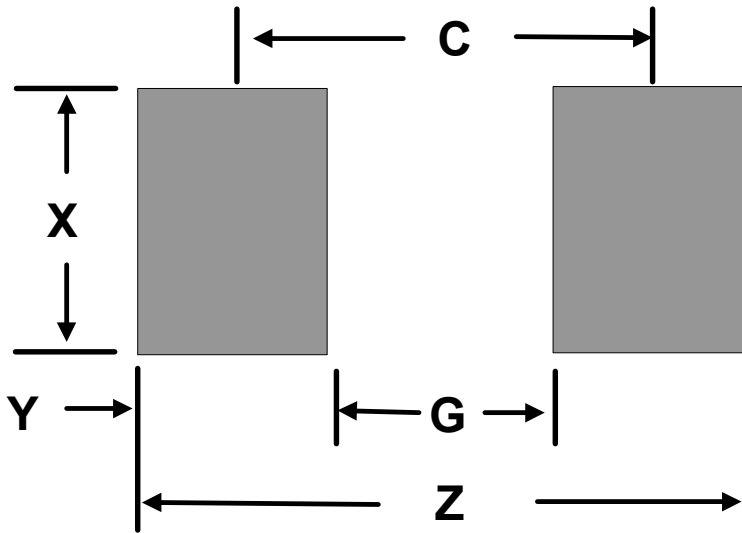
The volume of solder is process and board pad size dependent. WAVE SOLDERING exposes the devices to a large solder volume, hence the pad size area must be restricted to accept an amount of solder which is not detrimental to the chip size utilized. Typically the pad width is 66% of the component width, and the length is .030 (.760 mm) longer than the termination band on the chip. An 0805 chip which is .050 wide and has a .020 termination band therefore requires a pad .033 wide by .050 in length. Opposing pads should be identical in size to preclude uneven solder fillets and mismatched surface tension forces which can misalign the advice. It is preferred that the pad layout results in alignment of the long axis of the chips at right angles to the solder wave, to promote even wetting of all terminals. Orientation of components in line with the board travel direction may require dual waves with solder turbulence to preclude cold solder joints on the trailing terminals of the devices, as these are blocked from full exposure to the solder by the body of the capacitor.

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BOARD DESIGN CONSIDERATIONS (continued)

Restrictions in chip alignment do not apply to SOLDER REFLOW or VAPOR PHASE processes, where the solder volume is controlled by the solder paste deposition on the circuit pads. Pads are designed to match or slightly exceed the width of the capacitor, with length .030 (.760 mm) greater than the chip terminal band width, to provide a wetting area for a full solder fillet. The Institute for Interconnecting and Packaging Electronic Circuits (IPC) has developed and published IPC-SM-782A "Surface Mount Design and Land Pattern Standard." This standard presents industry consensus on optimum dimensions based on empirical knowledge of fabricated land patterns. It is highly recommended that the PCB designer/SMT process engineer obtain a complete copy of the standard.

RECOMMENDED PAD DIMENSIONS

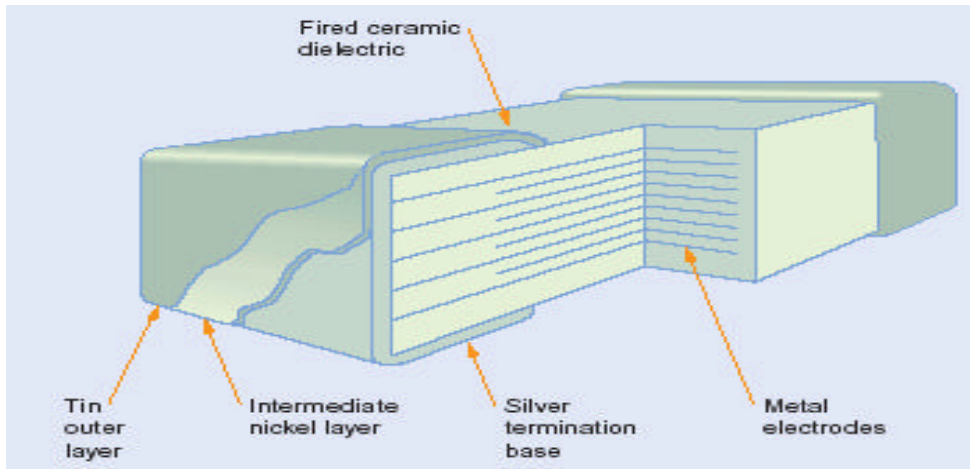


SIZE	Z	G*	X	Y(ref)	C(ref)
1808	.230" (5.84 mm)	.130" (3.30 mm)	.090" (2.29 mm)	.050" (1.27 mm)	.180" (4.57 mm)
1812	.230" (5.84 mm)	.130" (3.30 mm)	.135" (3.43 mm)	.050" (1.27 mm)	.180" (4.57 mm)

* IPC recommend the space be a minimum of .080".

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INSIDE STRUCTURE AND MATERIALS



NAME	MATERIAL
Ceramic Dielectric	SrTiO ₃ or BaTiO ₃
Metal Electrodes	Ag/Pd
Silver termination	Ag
Nickel layer	Ni
Tin layer	Sn

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