



Applications-Information 02/2014

Bend it, shape it, don't break it

Multilayer ceramic chip capacitors are renowned for their reliability but can be vulnerable to cracks when affected by PCB flexing. The resulting damage may not manifest itself immediately, but may ultimately result in field failure. Syfer Technology has introduced a polymer termination to its range of Multilayer Capacitors to permit greater degrees of board bending without damage to capacitors.



The multilayer ceramic chip capacitor is the capacitor of choice for surface mount applications.

There are generally three dielectric categories available; C0G [NP0], X7R and Y5V. Sizes usually range from 0201 (0.5mm long x 0.25mm wide) to 2225 (5.6mm long x 6.4mm wide).

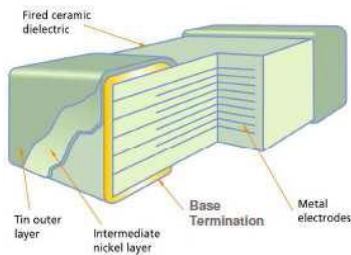
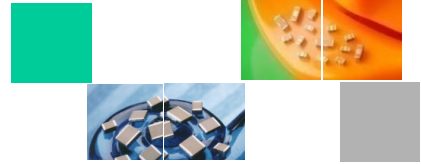


Figure 1 Multilayer Chip Capacitor Structure

A multilayer ceramic chip capacitor is a small block of ceramic dielectric material with embedded layers of metal. Those electrode layers are connected into a parallel plate structure by 'caps' of metallisation, terminations, applied to opposite ends of the block. (see figure 1).

It is one of the most reliable components for surface mount applications but it can fail due to fracture as a result of a PCB bending.



Applications-Information 02/2014



When a circuit board is deflected, it attempts to form an arc. The outer surface of the board stretches, increasing the distance between the solder lands on which the chip is mounted. This places the chip under tension, as shown in figure 2. Whilst the solder joint will be deformed, the chip may crack.

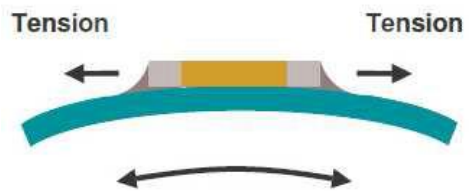


Figure 2 Board Bending May Break Chip Capacitors

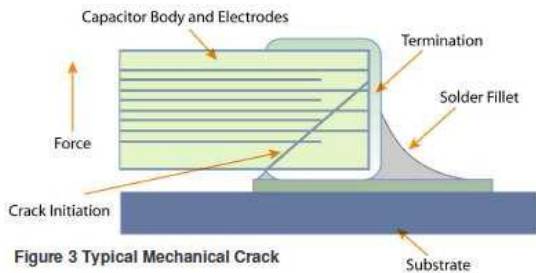


Figure 3 Typical Mechanical Crack

Figure 3 shows that the of the PCB bending is contained within the terminated area of the chip, running from the lower edge of the termination towards the end face. Should it enter the area of electrode overlap, an electrical short circuit may result.

The fault may not be detected until a long time after the fracture occurs. An immediate change in any key electrical parameter is rare when chips are broken. See figure 4.

However, a decline in the Insulation Resistance (IR) of the chip may be delayed until the cracked structure is penetrated by a conductive medium such as atmospheric moisture.

On individual boards, the electrical problem may be transient. As a result of thermal treatment, often applied inadvertently, the board may function only to fail again, some time later.

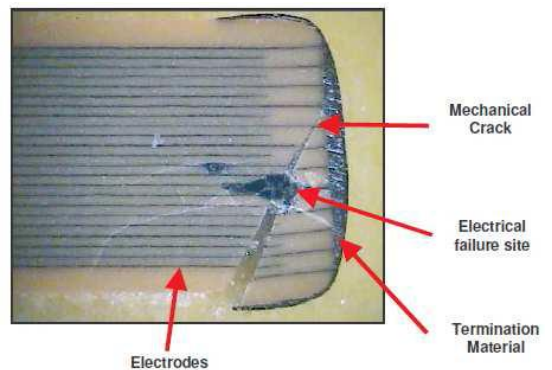
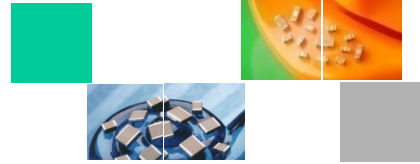


Figure 4 Electrical Short Circuit as a Result of Mechanical Fracture



Applications-Information 02/2014

While the board manufacturer will isolate the problem to a single capacitor, more sophisticated analysis may reveal that many other capacitors on the board have also cracked but have yet to affect board operation.

Typically, in analysing field failures around 60% of damaged parts exhibit a detectable change in IR but only a small minority of these are pre-identified as potential failures by a user. A change of capacitance value is a feature of no more than about 10% of cracked chips and cracks will be visible at the exterior of less than 2% of affected parts.

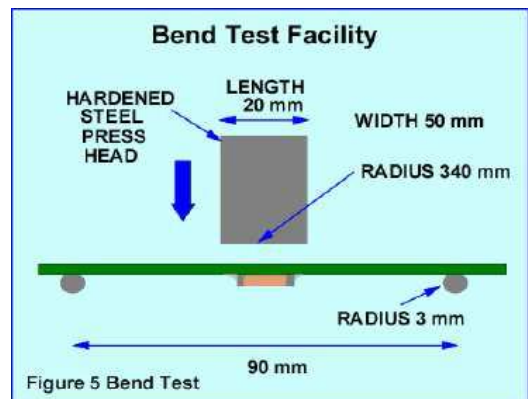
Board designers can take countermeasures to reduce a board's vulnerability to fracture. Most fractures occur at depanelisation, the separation of daughterboards from motherboards. Depanelisation should only be performed using purpose-built jigs and never by hand.

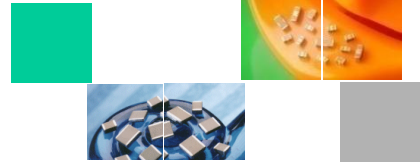
The possibility of so-called transient incidents, i.e. the use of 'uncontrolled' procedures, should also be recognised. Changing the source of capacitors might appear to solve the problem but, in that event, the circuit manufacturer will have failed to identify a true root cause and that 'oneoff occurrence' will inevitably happen again.

Based upon an analysis of field failures, no case can be made that any one size of chip is more vulnerable to failure by cracking than another. One factor does stand out, however, COG capacitors seldom feature in 'cracking incidents'.



A 'bend test' can evaluate chip strength. Figure 5 shows how chip capacitors are soldered to a test board, which is inverted over a pair of horizontal support rods. The board is deflected at a given speed, to a fixed extent, and an assessment of the effect on the capacitor, is made.





Applications-Information 02/2014

Syfer conducted a structured Bend Test programme, to determine the important parameters that affect a chip's ability to withstand bending forces. Some of the results obtained reinforced information already in the public domain while other results conflicted.

The most common electrical parameter employed as a measure of failure during a bend test is change of capacitance value. However, change of this parameter is seldom a feature of 'real incidents'. Recognising this, micro-sectioning was adopted as the key evaluation parameter for the programme, during which more than 15,000 chip capacitors were 'bent' and micro sectioned.

An immediate change of IR was observed in less than 1% of parts subsequently determined to have cracked.

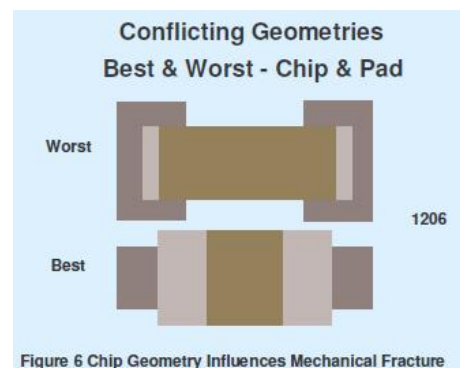
Correlating the failures determined by micro-section, with those suggested by capacitance measurement, it was clearly demonstrated that capacitance change was a feature of only a proportion of 'broken' parts.

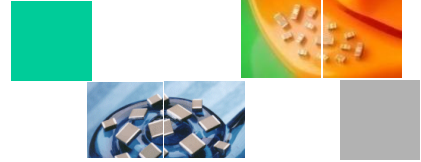
Small capacitors proved no stronger than large capacitors and thin capacitors were no weaker than thick capacitors, dispelling the myth that capacitor manufacturers could make parts stronger by making them thicker.

Results from the programme demonstrated that the only significant difference in strength, across a broad matrix of capacitor design and build parameters, lies between Barium Titanatebased components (the key material used in the X7R and Y5V dielectric categories) and Neodymium Oxide based components (the base material of the C0G [NP0] category).

C0G [NP0] capacitors fail at bend deflections approximately double those at which similar X7R and Y5V parts fail.

Circuit board solder pad design formed an important part of the programme. It was confirmed that land widths narrower than the chip width elevate bend strength significantly. See figure 6.





Applications-Information 02/2014

Similarly, the position of the edge of the termination band relative to the edge of the solder pad is a factor. If the capacitor termination edges are positioned 'inboard' of the solder lands, the assembly will withstand greater deflection without damage. The impact of the solder joint was examined. When the performance of a 'soft' solder, 50In 50Pb, as opposed to the more commonly used 62Sn 36Pb 2Ag, was checked the results were impressive. Average deflection at failure was more than doubled. The influence of the type of solder used upon the degree of chip fracture is a caution to those exploring the use of alternative, lead free formats that may be less elastic than the high lead-content materials.

This result illustrates that a chip assembly is a chain of materials -board, land, solder joint, chip termination and chip ceramic. Under tension, the weakest link fails and, in most instances, this is the ceramic. Compliance, in any link, would result in a stronger system.

While compliance on the part of the ceramic is impossible, it might be obtained from other materials in the chain.

Such an approach was adopted when working with suppliers of termination materials, substituting a conductive plastic for the glass-based conductor materials in common use.

This new termination is a silver-loaded epoxy polymer. It is flexible and it can reduce the stress between the PCB and the ceramic capacitor. The material is applied using conventional termination techniques, but instead of being sintered at approximately 800°C, the polymer is cured at 180°C.



Syfer's polymer termination has a fibrous structure and its mechanical and electrical properties remain largely unaffected by extremes of heat and chemical treatments (see figure 7).

After the polymer termination process stage, the capacitors are plated with Nickel and Tin using the same methods employed for industry standard sintered Silver-terminated capacitors so their soldering characteristics are unchanged.

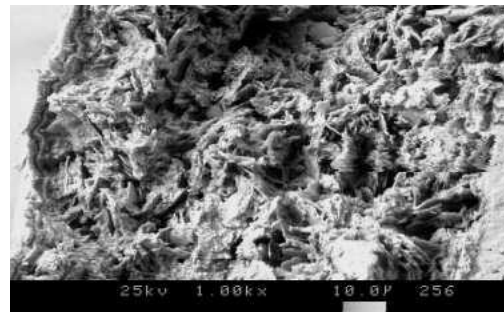
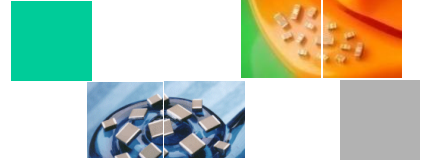


Figure 7 Polymer Termination Microstructure



Applications-Information 02/2014

The electrical parameters of a polymer-terminated chip are indistinguishable from a conventional part. Extensive reliability testing has confirmed that the polymer has no negative effect on electrical or environmental performance.

Typically, a polymer-terminated X7R or Y5V capacitor will afford a bend test deflection at failure, which is almost double that of the same capacitor with a conventional termination. This puts them at the same level as C0G [NP0] capacitors from which 'real life' failures are almost unknown.

Some 10 million polymer terminated X7R capacitors were supplied to customers for evaluation. The applications targeted were those known to have a long history of problems due to capacitor cracking.

During the course of these trials, not a single part was identified to have failed as a result of chip fracture.

These products are now available from Syfer as FlexiCap™ . They permit a much greater degree of board bending than conventional capacitors.



innovative, world-class
ceramic components





Applications-Information 02/14

Erweiterung des Produkt- & Herstellerportfolios



Leiterplattensteckverbinder, I/O Steckverbinder,
RF Steckverbinder, Rundsteckverbinder, Fiber Optic



Leiterplattensteckverbinder, I/O Steckverbinder,
Schalter, IC- Fassungen.



Leistungswiderstände, Drahtwiderstände,
Drahtdrehwiderstände,
Kleinleistungswiderstände, Sonderbauformen.



Trimming Potentiometers,
Chip- and Dipped Tantalum Capacitors



Printtransformatoren 50/60Hz; Leistung: 0,35VA bis
30KVA Standard, kundenspezifische Lösungen.

Impressum

Herausgeber: wts // electronic components GmbH
Langer Acker 28, 30900 Wedemark
Telefon +49 (0)5130 / 58 45 0
Telefax +49 (0)5130 / 37 50 55
www.wts-electronic.de info@wts-electronic.de